REMARKS

Applicant thanks Examiner for the detailed review of the application.

Claim Rejections -35 USC § 102(b)

The Office Action has rejected Claims 1-7, 12, 16, 19, 21, 24-26, 28, 29, 37-41, 46, and 53, under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,871,275 to Poplingher et al. (referred to hereinafter as "Poplingher"). However, the Office Action has failed to make a prima facie case of anticipation for the claims.

"[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ..." MPEP 706.02 (emphasis added). "The identical invention must be shown *in as complete detail as contained in the ... claim.*" *Richardson v., Suzuki Motor Co.*, 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Poplingher only discloses pre-fetching from a branch target address specified in a first instruction, i.e. a PTB instruction (see col. 3 lines 20-22). Next, it is decided if a branch is to be taken utilizing a separate and distinct second instruction, i.e. a CMP instruction (see col. 3 lines 21-24). Furthermore, Poplingher discloses storing the branch target address from the PTM instruction in a first register, i.e. an SBR file (see col. 4 lines 22-23). Then, based on the results of the branch prediction utilizing the CMP instruction, the target address is sent to a fetch unit to begin fetching if the branch is to be taken and the target address is disregarded if the branch is not to be taken (see col. 4 lines 42-52).

In contrast, applicant's claim 1 includes, "a first register to hold an incoming value…a predicated instruction that references at least the first register…a first micro-operation, when executed, to associate a predicate value with the incoming value in the second storage element; … and a third micro-operation, when executed, to update the first register with the incoming value in response to the predicate value representing a first value," (claim language redacted). Note that Poplingher only stores a target address in a single SBR or BR, where in applicant's claim 1 an incoming value held in the first register is moved to a second register and the incoming value is restored to the first register in response to the predicate value representing a first value, such as the predicate is true or false. In Polingher's disclosure if a branch is taken, the target address is simply forwarded to a fetch unit, and if the branch is not taken, the target address is disregarded. However, Poplingher does not disclose associating an incoming value, which was held in a first register, with a predicate value in a second register, placing a new value in the first register, and updating the first register with the incoming value in response to a predicate value, as in one embodiment of applicant's claim 1.

Applicant's claim 19 includes the element, "a select micro-operation to select the first or second value to be held in the first destination register based on the predicate value associated with the first value." As stated above, Poplingher only suggests providing a target address to a fetch unit or disregarding the target address based on a nomination pointer value, i.e. when a branch is taken or not taken, not selecting between a first or a second value to be held in a single register, i.e. the first destination register, as in applicant's claim 19.

Similarly, applicant's claim 24 includes the element, "generating a third operation, when executed, to select between the first value and the new value to be held in the first destination register." As stated above, Poplingher only teaches fetching or not fetching from a target address in a register based on whether a branch is taken, not selection between values to be held in the register itself.

In addition, the office action rejected claim 30 under 35 U.S.C. § 103(a) as being unpatentable over Poplingher in view of Examiner's use of Official Notice. However, applicant's claim 30 includes the element, "a third micro-operation to select the first value or the second value to be stored in the second destination register based on a predication value." As Poplingher does not disclose selecting between values to hold in a destination register, as stated above, and official notice of such would be improper, applicant respectfully submits that claim 30, as well as its dependent claims are in condition for allowance for at least the reasons stated above.

Therefore, applicant respectfully submits that independent claims 1, 19, 24, and 30, as well as their dependent claims, are in condition for allowance for the reasons stated above.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
Intel Corporation

Dated: June 16, 2008

/David P. McAbee/Reg. No. 58,104
David P. McAbee
Reg. No. 58,104

Intel Corporation
M/S JF3-147
2111 NE 25th Avenue
Hillsboro, OR 97124
Tele – 503-712-4988
Fax – 503-264-1729